Remarks

Upon entry of the foregoing amendment, claims 24-45 are pending in the application, with 24, 39, and 45 being the independent claims. Claim 1 is sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 24-45 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

The specification was amended in conformance with amendments made in the two previous above-mentioned applications and to add continuation data and more clearly discuss the invention. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided. Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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Version with markings to show changes made

The paragraph on Page 1, lines 7-10, is replaced with the following new paragraph:

--This application is a continuation of application Serial No. 09/649,197, filed August 28, 2000, now Patent 6,326,852, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, which is a continuation of 09/398,101, filed September 16, 1999, now Patent 6,181,210, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, and which is related to provisional application Serial No. 60/101,555, filed September 21, 1998, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP DESIGN, which are all commonly owned by the Assignee of the present invention.--

The paragraph beginning on Page 2, line 27, and ending on Page 3, line 8, is replaced with the following new paragraph:

--The data signal is received at a data input of the phase detector 10, in which the occurrence of the data's rising edge (its phase) is compared in time to the occurrence of a rising edge (the phase) of an output signal of the VCO 14. Conventionally, the phase detector incorporates logic circuitry [circuity](in effect a logical XNOR function) which precludes an output signal from being issued during phase comparisons unless two rising edges are present during a comparison cycle. This feature [features] prevents the phase-lock-loop from becoming unstable by trying to perform a phase comparison between a VCO rising edge and a DATA ZERO bit (necessarily without a rising edge). It will be understood that the phase comparison result in such a situation would indicate either an infinite phase lead or an infinite phase lag, thus causing the VCO frequency to run out of control.--

The paragraph being on Page 3, line 9 and ending on line 28 is replaced with the following new paragraph:

--According to convention, the phase detector 10 issues a PUMP UP signal 16 to the charge pump 12 if the datastream phase leads the VCO signal, and issues a PUMP DN 18 if the datastream phase lags the VCO signal. PUMP UP and PUMP DN are directed to the charge pump 12 which sources or sinks a particular amount of current (the pump current) to or from, respectively, the loop filter 13. Voltage is developed as the -pump current is sourced or sunk, with the voltage being used to control the operational frequency of the VCO 14. The sign of the VCO control voltage variation depends on whether the phase of the datastream leads or lags the phase of the VCO output and its magnitude is a function of the extent of the phase lead or phase lag. Thus, the operational frequency of the VCO 14 is increased or decreased, as appropriate, to reduce the phase lead or phase lag of the inputs to the phase detector 10. The phase-lock-loop thus ensures that the VCO output, which is used as a timing reference, is locked in phase with the incoming serial datastream. Once the PLL is "locked", the timing reference signal (i.e., the VCO output) is used to control operation of a decision circuit 19 [16] which defines regenerated or retimed data.--

The paragraph beginning on Page 9, line 3 and ending on line 12 is replaced with the following new paragraph:

--In practical terms, lack of perfect symmetry between sourced and sunk charge pump current selectively adds a small component (a DC offset component, a glitch error component, or both) to the control voltage Vc provided to a VCO. These error components selectively shift frequency of a VCO relative to its nominal center frequency. Any offset from the center frequency will cause a phase detector's data capture window to shift, thus allowing a portion of data pulse position distribution to fall outside [out side] the detection window, and consequently increasing the system's bit error rate.--

The paragraph beginning on Page 11, line 28, through Page 12, line 4, is replaced with the following new paragraph:

--Similarly, the second current path, the right current path, is constructed of an upper P-channel transistor 50 and a lower N-channel transistor 52. The P-channel transistors 46 and 50 are mirror images of one another and have their source [drain] terminals connected together in common and to the pump-up current source 42. The lower N-channel transistors 48 and 52 are likewise mirror images of one another and also have their source terminals connected in common to the pump-down current source 44.--

The paragraph beginning on Page 12, line 23 and ending on line 30 is replaced with the following new paragraph:

--An output node is defined by the common drain nodes of the P-channel and N-channel transistors defining one of the parallel current paths. Source and sink currents are output to an analog loop filter 54 constructed to include an RC network characterized by a resistor element 56 and a capacitor 58 which define the filter's [filters] zero. The RC network is coupled between the charge pump output and ground in parallel with a second capacitor 60 which defines the analog loop filter's pole.--

The paragraphs beginning on Page 13, line 32 and ending on Page 14, line 20 are replaced with the following new paragraphs:

--Further, the transconductance amplifier 62 forces the common drain nodes of each of the current paths of the charge pump 40 to be maintained at an equi-potential value with respect to one another. Thus, transconductance amplifier in combination with the "adjust" current source 63 functions to force the "down" current sunk by the "down" current source 44 to exactly equal the "up" current sourced by the "up" current source 42, in a manner independent of the output voltage of the charge pump. Thus, any DC mismatches between the "up" and "down" current sources which could cause offsets in the charge pump output, are removed. Since the charge pump output nodes are maintained at an equi-potential level, there is no further voltage dependence of the "up" and "down" current sources on the output voltage and (further minimized) DC offsets in the charge pump output are minimized.

It should be realized by one having skill in the art that the third [thrid] "adjust" current source 63 need not be provided [n]either as a separate element[, n]or in parallel with the "down" current source 44. In alternative embodiments, [T]the "adjust" current source may receive a signal from the amplifier 62 and may [might also] be partially or wholly provided in parallel with the "pump-up" current source 42. In still other configurations [Further,] the "adjust" current source 63 might be eliminated as a separate element and the amplifier 62 may be configured to control either the "pump-up" 42 or "pump-down" 44 current sources directly.--

The paragraph beginning on Page 15, line 16 and ending on line 22 is replaced with the following new paragraph:

--It will thus be recognized by those skilled in the art that various modifications may be made to the illustrated and other embodiments of the invention described above, without [with out] departing from the broad inventive scope thereof. It will be understood, therefore, that the invention is not limited to the particular embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as defined by the appended claims.